

Version 3.1	Course Academic Plan	Course Code and Name: ITC405 Computer Organization and Architecture
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The academic resources available in PHCET, Rasayani

PHCET AMS	Evaluation and Assessment	PHCET Library	Value added courses and MOOC courses
Institute & Department Vision and Mission	Former IA question papers and solutions (prepared by faculty)	Former IA question papers solutions - hardcopy	Value Added Courses (VAC) are conducted throughout the semester & in the semester break -
Lesson Plan, Practical plan, Content delivery (Planned and Actual)	MU end semester examination question papers and solutions (prepared by faculty)	MU end semester exam question paper & solutions - by faculty, hardcopy	Online courses from NPTEL, Coursera etc. are pursued throughout the semester
Student attendance and performance	Class notes and Digital Content for the subject	All text books, reference books, e -books mentioned in the syllabus & AAP	Video recording of Lectures captured in Light board studio at PHCET is made available.
Student details	Comprehensive question bank, MCQ, GA, PPT, Class Test papers	Technical journals and magazines for reference	Interactive smart board facility is available and lectures are recorded.
Departmental Academic plan	Academic Administration Plan & Beyond Syllabus Activity report	PHCET library is member of IIT Bombay Library	Expert lectures by Industry/Academia

1. a Course Objectives (As per Blooms Taxonomy)

Sr No	Course Objectives
1	Learn the fundamentals of Digital Logic Design.
2	Conceptualize the basics of organizational and features of a Digital computer.
3	Study microprocessor architecture and assembly language programming
4	Study processor organization and parameters influencing performance of a processor
5	Analyse various algorithms used for arithmetic operations. 6. Study the function of each element of memory hierarchy and various data transfer techniques used in digital computer.

1.b Course Outcome (CO) Mapping with Modules

Sr No	COs	Related Module/s
CO1	Demonstrate the fundamentals of Digital Logic Design	1
CO2	Describe basic organization of computer, the architecture of 8086 microprocessor and implement assembly language programming for 8086 microprocessors	2

CO3	Demonstrate control unit operations and conceptualize instruction level parallelism	3
CO4	List and Identify integers and real numbers and perform computer arithmetic operations on integers	4
CO5	Categorize memory organization and explain the function of each element of a memory hierarchy	5
CO6	Examine different methods for computer I/O mechanism.	6

1.c Mapping of COs with POs (mark 3: Strong, 2: Moderate, 1: Weak,)

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12
CO 1	1		.66		.33	.33			.66			
CO 2	.66	1	.66			.33					.33	
CO 3	1	.66	1		.33	.33	.33		.33			
CO 4	.66	.66	1		.33	.33		.33				
CO 5	1	.66	1		.33	.33	.33		.33			
CO 6	.66	.33		.33						.33		

1.d Mapping of COs with PSOs

CO	PSO 1	PSO 2	PSO 3	PSO 4
ITC405.1	1	.66	.33	.33
ITC405.2	1		.66	
ITC405.3		1	1	.33
ITC405.4	.33	.66	1	
ITC405.5	1	1	.33	
ITC405.6	1			

1.e Core Competency of the course

Categories	Mathematics	Basic Science & General Engg	Humanities & Soft Skill	Core Engg./ Technology - Design & Analysis	Multidisciplinary
Tick where applicable				✓	

2. a Teaching Scheme (As specified by the University)

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2. b Module Wise Teaching Hours and % Weightage in University Question Paper

Module No.	Module Title and Brief Details	Teaching Hrs. for each module	% Weightage in University Question Papers
1	Fundamentals of Logic Design	7	15
2	Overview of computer Architecture & Organization	8	17
3	Processor Organization and Architecture	7	15
4	Data Representation and Arithmetic Algorithms	4	09
5	Memory Organization	7	15
6	I/O Organization	4	09

2.c Prerequisite Courses

Sr. No.	Semester	Name of the course	Topics covered
1	III	Principal of Communication	1.Modulation 2.Multiple Techniques Access

2. d Relevance to Future Courses

Sr. No.	Semester	Name of the course

2. e Industry Application of the course

Sr. No	Application
1	Designing any type of Enterprise

3.a Past Results –

	Division A		Division B		Division C	
Year	Initials of Teacher	% Result	Initials of Teacher	% Result	Initials of Teacher	% Result

Topics which affect results negatively	Module Number	Recommendations to overcome these issues & improve result in future

4. a Learning Resources – Books and E-Resources

4. b List of Text Books

- T1. R. P. Jain, "Modern Digital Electronics", TMH
T2. M. Morris Mano, "Digital Logic and Computer Design", PHI
T3. Carl Hamacher, Zvonko Vranesic and Safwat Zaky, Computer Organization, Fifth Edition, Tata McGraw-Hill.
T4. William Stallings, Computer Organization and Architecture: Designing for Performance, Eighth Edition,, Pearson
T5. John Uffenbeck, 8086/8088 family: Design Programming and Interfacing, (Pearson Education)

4. c List of Reference Books

- R1. A. Anand Kumar, "Fundamentals of Digital Circuits",. PHI
R2. Donald P Leach, Albert Paul Malvino, "Digital Principals & Applications", TMH. R3. B. Govindarajulu,, Computer Architecture and Organization: Design Principles and

Applications, Computer Architecture and Organization: Design Principles and Applications, Tata McGraw-Hill

R4. Dr. M. Usha, T. S. Srikanth, Computer System Architecture and Organization, First Edition, Wiley-India. R5. John P. Hayes, Computer Architecture and Organization, Third Edition., McGraw-Hill R6. K Bhurchandi, “Advanced Microprocessors & Peripherals”, Tata McGraw-Hill Education

4.d List of E – Books

4.e Web Links and Names of Magazines, Journals, E-journals

Sr. No.	Web-Links and Names of Journals and E-Journals Recommended	Web-Links and Names of Magazines Recommended	Module Nos.

Sr. No	Module	Detailed Content	Hours	CO Mapping Referer	
0	Prerequisite	Basics of Electrical Engineering, Fundamentals of Computer	02		
1	Fundamentals of Logic Design	<p>Number systems: Introduction to Number systems, Binary Number systems, Signed Binary Numbers, Binary, Octal, Decimal and Hexadecimal number and their conversions, 1's and 2's complement.</p> <p>Combinational Circuits: NOT,AND,OR,NAND,NOR,EX-OR,EX-NOR Gates. , Reduction of Boolean functions using K-map method (2,3,4 Variable), Half& Full Adder and subtractor, introduction to Multiplexers and Demultiplexers, Encoders & Decoders.</p> <p>Sequential Circuits: Introduction to Flip Flops: SR, JK, D, T, master slave flip flop, Truth Table.</p>	07	CO1	T1,T2,R1,R2

		Self-learning Topics: Number System, Quine-McCluskey, Flip-Flop conversion, Counter Design.			
2	Overview of computer Architecture & Organization	<p>Introduction of Computer Organization and Architecture. Basic organization of computer and block level description of the functional units. Evolution of Computers, Von Neumann model. Performance measure of Computer Architecture, Amdahl's Law</p> <p>Architecture of 8086 Family- Instruction Set, Addressing Modes, Assembler Directives, Mixed-Language Programming, Stack, Procedure, Macro.</p> <p>Self-learning Topics: Interfacing of I/O devices with 8086(8255, ADC, DAC).</p>	08	CO2	T4, T5, R4
3	Processor Organization and Architecture	<p>CPU Architecture, Instruction formats, basic instruction cycle with Interrupt processing. Instruction interpretation and sequencing. Control Unit: Soft wired (Microprogrammed) and hardwired control unit design methods. Microinstruction sequencing and execution. Micro operations, concepts of nano programming. Introduction to parallel processing concepts, Flynn's classifications, instruction pipelining, pipeline hazards.</p> <p>Self-learning Topics: Study the examples on instruction pipelining for practice.</p>	07	CO3	T3, T4, R5
4	Data Representation and Arithmetic Algorithms	Booth's algorithm. Division of integers: Restoring and non-restoring division, signed division, basics of floating-point representation IEEE 754 floating	04	CO4	T4, R5

		point (Single & double precision) number representation. Self-learning Topics: Implement Booth's Algorithm and Division methods.			

5	Memory Organization	Introduction to Memory and Memory parameters. Classifications of primary and secondary memories. Types of RAM and ROM, Allocation policies, Memory hierarchy and characteristics. Cache memory: Concept, architecture (L1, L2, L3), mapping techniques. Cache Coherency, Interleaved and Associative memory Self-learning Topics: Case study on Memory Organization, Numerical on finding EAT, Address mapping.	07	CO5	T4
6	I/O Organization	Input/output systems, I/O module-need & functions and Types of data transfer techniques: Programmed I/O, Interrupt driven I/O and DMA Self-learning Topics: Comparison of all I/O methods.	04	CO6	T5

Text Books:

- T1. R. P. Jain, "Modern Digital Electronics", TMH
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R4. Dr. M. Usha, T. S. Srikanth, Computer System Architecture and Organization, First Edition, Wiley-India. R5. John P. Hayes, Computer Architecture and Organization, Third Edition., McGraw-Hill R6. K Bhurchandi, “Advanced Microprocessors & Peripherals”, Tata McGraw-Hill Education

6.0 Web Links for Online Notes/YouTube/ Digital Content/Lecture Capture/NPTEL Videos

Sr. No.	Websites/ Links	Module No
1.	https://youtu.be/nxryfWg5Hm4	1
2.	https://youtu.be/_83U55XBIXg	1
3	https://youtu.be/fn9Hn_x6dA	5
4	https://youtu.be/ltvpkuQRZao	6
5		

7. Recommended MOOC Courses like Coursera / NPTEL / Swayam/ edX etc.

Sr. No.	MOOC course link	Resource Person	Course duration	Certificate (Y/N)
1	Microprocessor and its applications	Coursera	8 weeks	
2	Microprocessor and microcontrollers	NPTEL	4weeks	

8. Study Material Distributed among Students

GA	Notes (Hand Written)	Digital content	PPT	MCQ	Other

9. Lesson Plan

Week	Lecture no.	Module No.	Lecture Topics / IA 1 and IA 2 / BSA planned to be covered	Actual date of Completion	Mapping with COs	Recommended Prior Viewing / Reading	
						Lecture No. (on LMS)	Chapter No. / Page Nos./ Books/ Web Site

10. Rubric for Grading and Marking of Term Work

Lecture + Practical (% Attendance) & Marks	Assignments	Tutorial	Lab / Practical Performance J\ [ouytrew6e5wq	Lab Journal Assessment	Mooc Course	Total

11. Practical/Assignment Plan

Practical/Assignment No.	Module no.	Title of experiment/assignment	Mapping with Cos
1	1,2,3,4,5	2. Virtual Lab http://vlabs.iitb.ac.in/vlabs-dev/labs/digital_electronics/experimentlist.html 3. GUI Turbo Assembler(TASM) https://sourceforge.net/projects/guitasm8086/	1,2,3,4,5,6

12. Beyond Syllabus Activities for Gap Mitigation

No	Type of the Activity	Activities	Details – no of attendees, guest, feedback, mark sheet, report

Academic Plan prepared by

Name of Faculty: Dr.Divya Y.Chirayil
Sign:

Domain Co-ordinator	SIG Coordinator	HOD